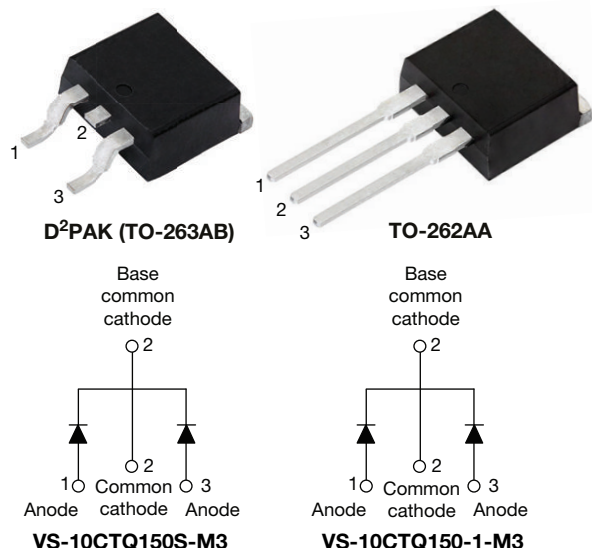


High Performance Schottky Rectifier, 2 x 5 A



FEATURES

- 175 °C T_J operation
- Center tap configuration
- Low forward voltage drop
- High frequency operation
- High purity, high temperature epoxy encapsulation for enhanced mechanical strength and moisture resistance
- Guard ring for enhanced ruggedness and long term reliability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 245 °C
- Designed and qualified according to JEDEC®-JESD 47
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

DESCRIPTION

This center tap Schottky rectifier has been optimized for low reverse leakage at high temperature. The proprietary barrier technology allows for reliable operation up to 175 °C junction temperature. Typical applications are in switching power supplies, converters, freewheeling diodes, and reverse battery protection.

PRIMARY CHARACTERISTICS

I _{F(AV)}	2 x 5 A
V _R	150 V
V _F at I _F	0.93 V
I _{RM}	7 mA at 125 °C
T _J max.	175 °C
E _{AS}	5 mJ
Package	D ² PAK (TO-263AB), TO-262AA
Circuit configuration	Common cathode

MAJOR RATINGS AND CHARACTERISTICS

SYMBOL	CHARACTERISTICS	VALUES	UNITS
I _{F(AV)}	Rectangular waveform	10	A
V _{RRM}		150	V
I _{FSM}	t _p = 5 μs sine	620	A
V _F	5 A _{pk} , T _J = 125 °C (per leg)	0.73	V
T _J	Range	-55 to +175	°C

VOLTAGE RATINGS

PARAMETER	SYMBOL	VS-10CTQ150S-M3 VS-10CTQ150-1-M3	UNITS
Maximum DC reverse voltage	V _R	150	V
Maximum working peak reverse voltage	V _{RWM}		

**ABSOLUTE MAXIMUM RATINGS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum average forward current, see fig. 5	$I_{F(AV)}$	50 % duty cycle at $T_C = 155^\circ\text{C}$, rectangular waveform	5	A
per leg per device			10	
Maximum peak one cycle non-repetitive surge current per leg, see fig. 7	I_{FSM}	5 μs sine or 3 μs rect. pulse	620	A
		10 ms sine or 6 ms rect. pulse	115	
Non-repetitive avalanche energy per leg	E_{AS}	$T_J = 25^\circ\text{C}$, $I_{AS} = 1\text{ A}$, $L = 10\text{ mH}$	5	mJ
Repetitive avalanche current per leg	I_{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T_J maximum $V_A = 1.5 \times V_R$ typical	1	A

ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum forward voltage drop per leg See fig. 1	$V_{FM}^{(1)}$	5 A	0.93	V
		10 A	1.10	
		5 A	0.73	
		10 A	0.86	
Maximum reverse leakage current per leg See fig. 2	$I_{RM}^{(1)}$	$T_J = 25^\circ\text{C}$	0.05	mA
		$T_J = 125^\circ\text{C}$	7	
Threshold voltage	$V_{F(TO)}$	$T_J = T_J$ maximum	0.468	V
Forward slope resistance	r_t		28	m Ω
Maximum junction capacitance per leg	C_T	$V_R = 5\text{ V}_{DC}$ (test signal range 100 kHz to 1 MHz), 25°C	200	pF
Typical series inductance per leg	L_S	Measured lead to lead 5 mm from package body	8.0	nH
Maximum voltage rate of change	dV/dt	Rated V_R	10 000	V/ μs

Note(1) Pulse width < 300 μs , duty cycle < 2 %**THERMAL - MECHANICAL SPECIFICATIONS**

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNITS
Maximum junction and storage temperature range	T_J, T_{Stg}		-55 to +175	$^\circ\text{C}$
Maximum thermal resistance, junction to case per leg	R_{thJC}	DC operation	3.50	$^\circ\text{C/W}$
Maximum thermal resistance, junction to case per package			1.75	
Typical thermal resistance, case to heatsink (only for TO-220)	R_{thCS}	Mounting surface, smooth and greased	0.50	
Approximate weight			2	g
			0.07	oz.
Mounting torque	minimum		6 (5)	kgf · cm
	maximum		12 (10)	(lbf · in)
Marking device		Case style D ² PAK (TO-263AB)	10CTQ150S	
		Case style TO-262AA	10CTQ150-1	

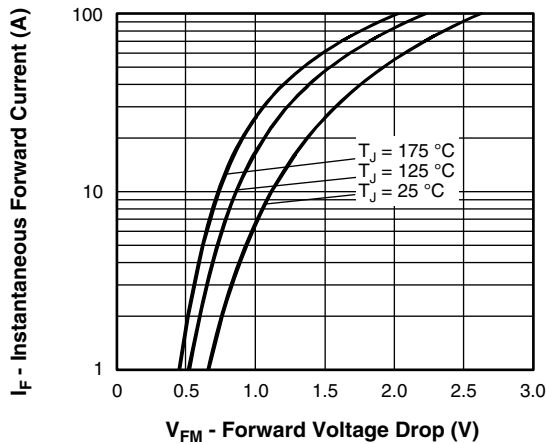


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

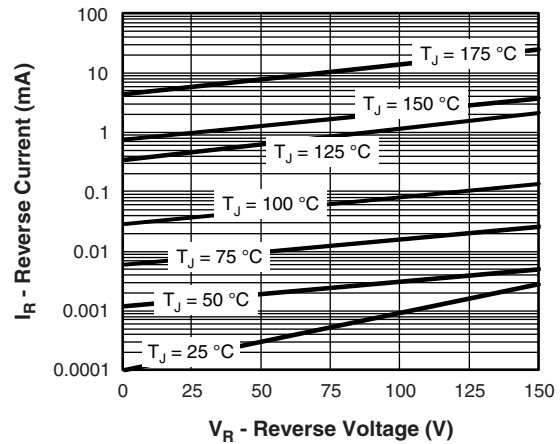


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

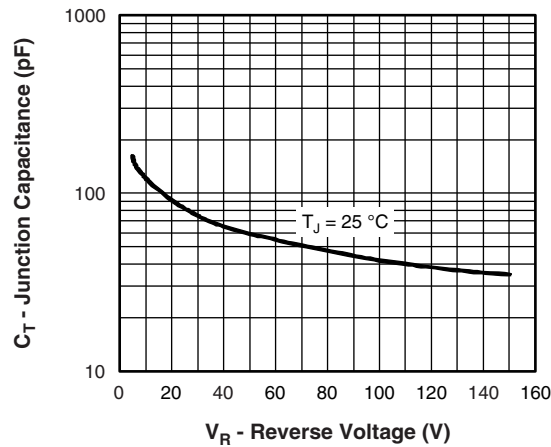


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

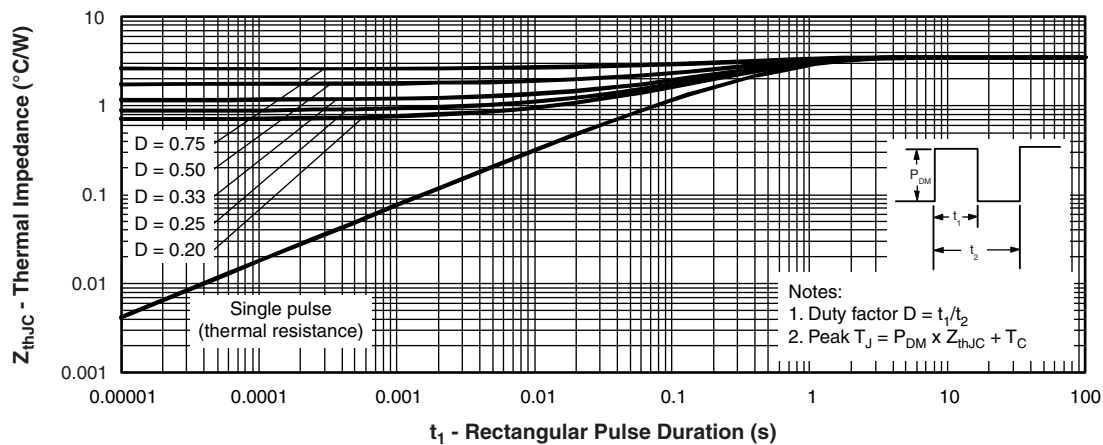


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics (Per Leg)

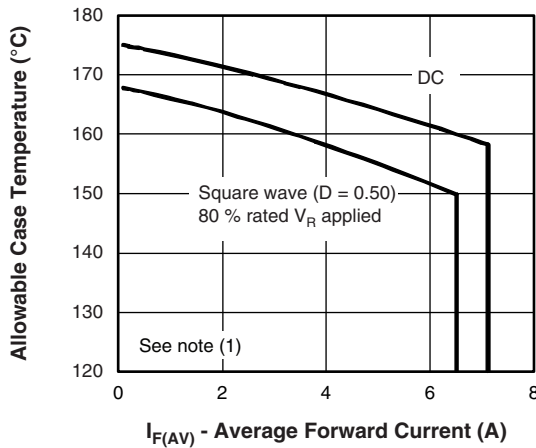


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

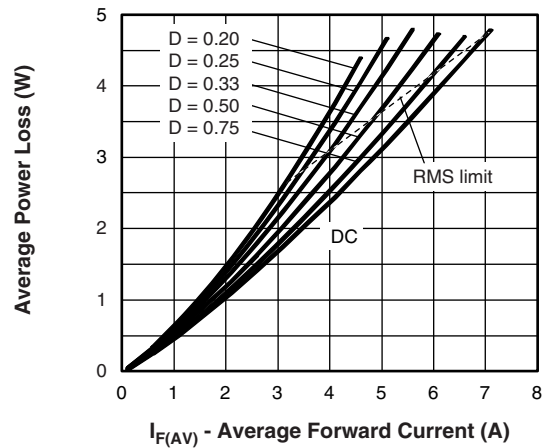


Fig. 6 - Forward Power Loss Characteristics (Per Leg)

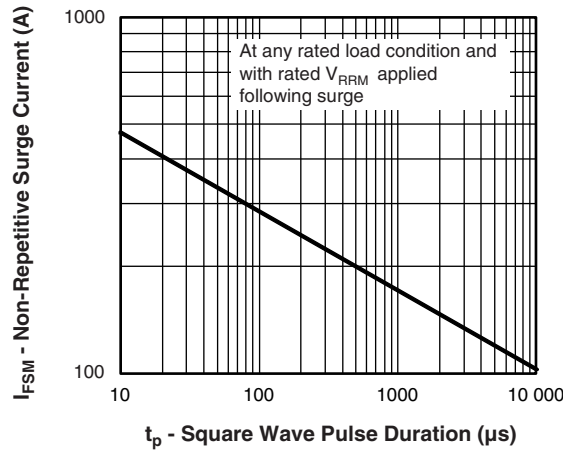


Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

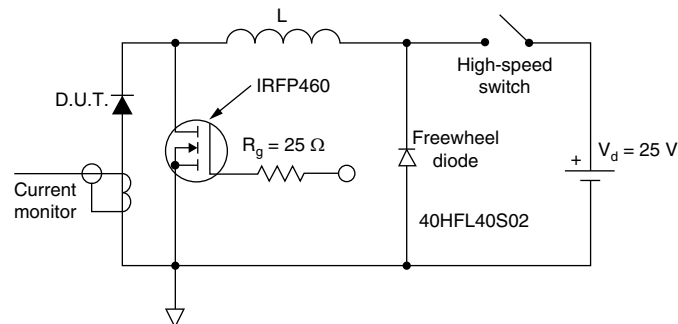


Fig. 8 - Unclamped Inductive Test Circuit

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{dREV}) \times R_{thJC}$;
 P_d = forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 P_{dREV} = inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 10\text{ V}$



ORDERING INFORMATION TABLE

Device code	VS-	10	C	T	Q	150	S	TRL	-M3
	1	2	3	4	5	6	7	8	9
1	Vishay Semiconductors product								
2	Current rating (10 A)								
3	Circuit configuration: C = common cathode								
4	T = TO-220								
5	Schottky "Q" series								
6	Voltage rating (150 = 150 V)								
7	• S = D ² PAK (TO-263AB) • -1 = TO-262AA								
8	• None = tube (50 pieces) • TRL = tape and reel (left oriented - for D ² PAK (TO-263AB) only) • TRR = tape and reel (right oriented - for D ² PAK (TO-263AB) only)								
9	-M3 = halogen-free, RoHS-compliant, and termination lead (Pb)-free								

ORDERING INFORMATION (Example)

PREFERRED P/N	BASE QUANTITY	PACKAGING DESCRIPTION
VS-10CTQ150S-M3	50	Antistatic plastic tubes
VS-10CTQ150STRL-M3	800	13" diameter plastic tape and reel
VS-10CTQ150STRR-M3	800	13" diameter plastic tape and reel
VS-10CTQ150-1-M3	50	Antistatic plastic tubes

LINKS TO RELATED DOCUMENTS

Dimensions	D ² PAK (TO-263AB)	www.vishay.com/doc?96164
	TO-262AA	www.vishay.com/doc?96165
Part marking information	D ² PAK (TO-263AB)	www.vishay.com/doc?95444
	TO-262AA	www.vishay.com/doc?95443
Packaging information		www.vishay.com/doc?96424



D²PAK

DIMENSIONS in millimeters and inches

Conforms to JEDEC® outline D²PAK (SMD-220)



SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	0.00	0.254	0.000	0.010	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
H	14.61	15.88	0.575	0.625	
L	1.78	2.79	0.070	0.110	
L1	-	1.65	-	0.066	3
L2	1.27	1.78	0.050	0.070	
L3	0.25 BSC		0.010 BSC		
L4	4.78	5.28	0.188	0.208	

Notes

- (1) Dimensioning and tolerancing per ASME Y14.5 M-1994
- (2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
- (3) Thermal pad contour optional within dimension E, L1, D1 and E1
- (4) Dimension b1 and c1 apply to base metal only
- (5) Datum A and B to be determined at datum plane H
- (6) Controlling dimension: inch
- (7) Outline conforms to JEDEC® outline TO-263AB

TO-262

DIMENSIONS in millimeters and inches

Modified JEDEC® outline TO-262

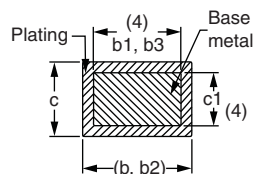
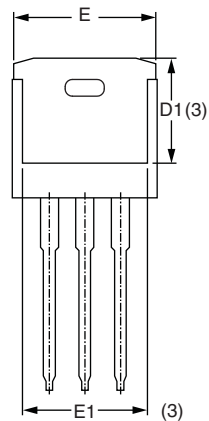
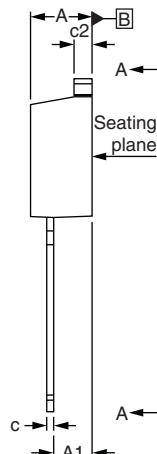


$\Phi 0.010 \text{ MAM} \text{ B}$



Lead assignments

- Diodes**
 1. - Anode (two die)/open (one die)
 2., 4. - Cathode
 3. - Anode



Section B - B and C - C
 Scale: None

SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	0.160	0.190	
A1	2.03	3.02	0.080	0.119	
b	0.51	0.99	0.020	0.039	
b1	0.51	0.89	0.020	0.035	4
b2	1.14	1.78	0.045	0.070	
b3	1.14	1.73	0.045	0.068	4
c	0.38	0.74	0.015	0.029	
c1	0.38	0.58	0.015	0.023	4
c2	1.14	1.65	0.045	0.065	
D	8.51	9.65	0.335	0.380	2
D1	6.86	8.00	0.270	0.315	3
E	9.65	10.67	0.380	0.420	2, 3
E1	7.90	8.80	0.311	0.346	3
e	2.54 BSC		0.100 BSC		
L	13.46	14.10	0.530	0.555	
L1	-	1.65	-	0.065	3
L2	3.36	3.71	0.132	0.146	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Dimension D and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outmost extremes of the plastic body
- (3) Thermal pad contour optional within dimension E, L1, D1 and E1
- (4) Dimension b1 and c1 apply to base metal only
- (5) Controlling dimension: inches
- (6) Outline conform to JEDEC TO-262 except A1 (maximum), b (minimum), D1 (minimum) and L2 where dimensions derived the actual package outline



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